Exhibit

7

# 27F256
# 256K (32K x 8) CMOS FLASH MEMORY

- **Flash Electrical Chip-Erase**
  - — 1 Second Typical Chip-Erase up to 10sec.
- **Quick-Pulse Programming™**
  - — 100 μs Typical Byte-Program
  - — 4 Second Chip-Program
- **EPROM-Compatible 12.75V $V_{PP}$ Supply**
- **100 Erase/Program Cycles**
- **High-Performance Speeds**
  - — 170 ns Maximum Access Time
- **Low Power Consumption**
  - — 100 μA Maximum Standby Current
- **Command Register Architecture for Microprocessor/Microcontroller Compatible Write Interface**
- **Noise Immunity Features**
  - — ±10% $V_{CC}$ Tolerance
  - — Maximum Latch-Up Immunity through EPI Processing
- **ETOX™ Flash-Memory Technology**
  - — EPROM-Compatible Process Base
  - — High-Volume Manufacturing Experience
- **Compatible with JEDEC-Standard Byte-Wide EPROM Pinouts**
  - — 28-Pin "Windowless" Cerdip

(See Packaging Spec., Order #231369)

Intel's 27F256 CMOS flash-memory offers the most cost-effective and reliable alternative for updatable non-volatile memory. The 27F256 adds electrical chip-erasure and reprogramming to familiar EPROM technology. Memory contents can be erased and reprogrammed: in a test socket; in a PROM-programmer socket; on-board during subassembly test; in-system during final test; and in-system alter-sale. The 27F256 increases memory flexibility, while contributing to time- and cost-savings. The 27F256 is targetted for alterable code- or data-storage applications where EPROM ultraviolet erasure is impractical or time consuming. The 27F256 can also be applied where traditional EEPROM functionality (byte-erasure) is either not required or not cost-effective.

The 27F256 is a 256-kilobit nonvolatile memory organized as 32768 bytes of 8 bits. Intel's 27F256 is offered in a 28-pin "windowless" cerdip package. Pin assignments conform to JEDEC standards for byte-wide EPROMs.

Intel's 27F256 employs advanced CMOS circuitry for systems requiring high-performance access speeds, low power consumption, and immunity to noise. Its 170 nanosecond access time provides no-WAIT-state performance for a wide range of microprocessors and microcontrollers. Maximum standby current of 100 microamps translates into power savings when the device is deselected. Finally, the highest degree of latch-up protection is achieved through Intel's unique EPI processing. Prevention of latch-up is provided for stresses up to 100 milliamps on address and data pins, from −1V to $V_{CC}$ + 1V.

With Intel's ETOX™ (EPROM tunnel oxide) process base, the 27F256 levers years of EPROM experience to yield the highest levels of quality, reliability, and cost-effectiveness.


Order Number: 290157-002

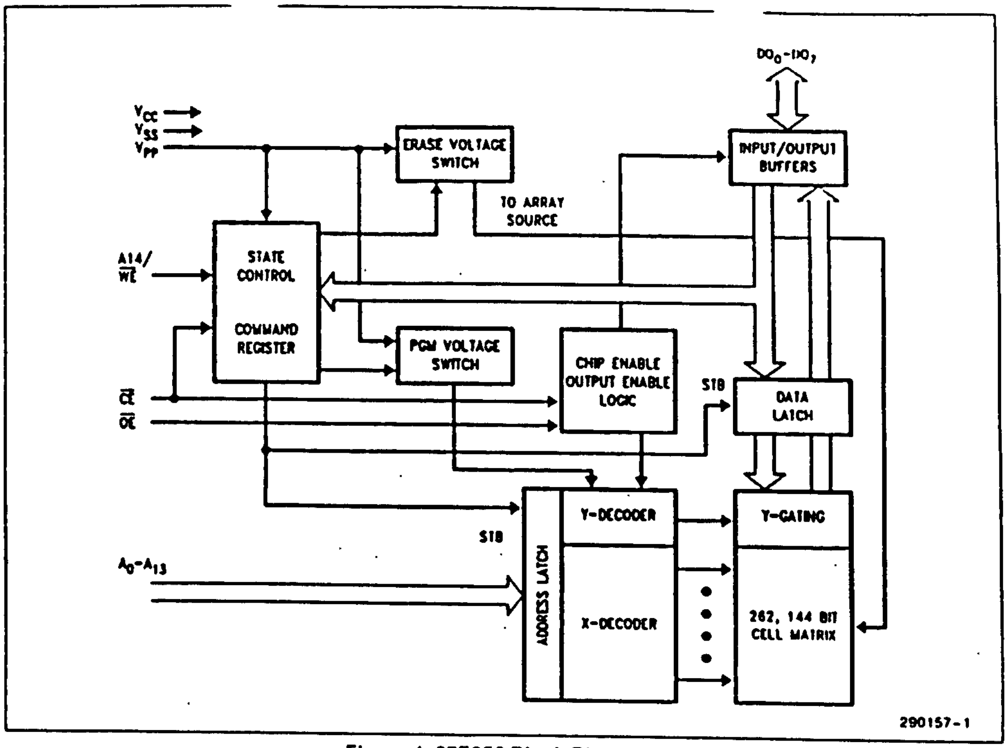


Figure 1. 27F256 Block Diagram

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| Sym |
|---|
| $A_0-A$ |
| $DQ_0-$ |
| $\overline{CE}$ |
| $\overline{OE}$ |
| $A_{14}/$ |
| $V_{PP}$ |
| $V_{CC}$ |
| $V_{SS}$ |

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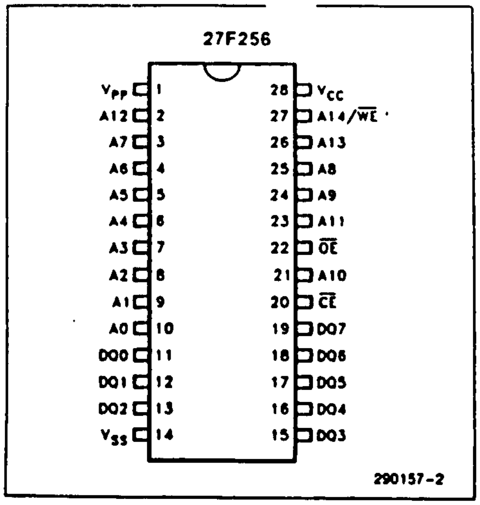


**Figure 2. Cerdip (D) Pin Configuration**

**Pin N[illegible]s**

| | |
|---|---|
| $A_0$–$A_{13}$ | Address Inputs |
| $DQ_0$–$DQ_7$ | Data Input/Output |
| $\overline{CE}$ | Chip Enable |
| $\overline{OE}$ | Output Enable |
| $A_{14}/\overline{WE}$ | Address/Write Enable |
| $V_{PP}$ | Program/Erase Power |
| $V_{CC}$ | Device Power |
| $V_{SS}$ | Ground |

**Table 1. Pin Description**

| Symbol | Type | Name and Function |
|---|---|---|
| $A_0$–$A_{13}$ | INPUT | **ADDRESS INPUTS** for memory addresses. Addresses are internally latched during a write cycle. |
| $DQ_0$–$DQ_7$ | INPUT/ OUTPUT | **DATA INPUT/OUTPUT:** Inputs data during memory write cycles; outputs data during memory read cycles. The data pins are active high and float to tri-state OFF when the chip is deselected or the outputs are disabled. Data is internally latched during a write cycle. |
| $\overline{CE}$ | INPUT | **CHIP ENABLE:** Activates the device's control logic, input buffers, decoders, and sense amplifiers. $\overline{CE}$ is active low; $\overline{CE}$ high deselects the memory device and reduces power consumption to standby levels. |
| $\overline{OE}$ | INPUT | **OUTPUT ENABLE:** Gates the device's output through the data buffers during a read cycle. $\overline{OE}$ is active low. |
| $A_{14}/\overline{WE}$ | INPUT | **ADDRESS/WRITE ENABLE** are multiplexed to maintain EPROM pinout compatibility. With $V_{PP}$ high, $A_{14}/\overline{WE}$ functions as the write control pin. With $V_{PP}$ low, $A_{14}/\overline{WE}$ functions as an address input line. $\overline{WE}$ is active low. Addresses are latched on the falling edge of $\overline{WE}$. Data is latched on the rising edge of the $\overline{WE}$ pulse. Note: With $V_{PP} = V_{PPL}$, memory contents cannot be altered. |
| $V_{PP}$ | | **ERASE/PROGRAM POWER SUPPLY** for writing the command register, erasing the entire array, or programming bytes in the array. |
| $V_{CC}$ | | **DEVICE POWER SUPPLY** (5V ± 10%) |
| $V_{SS}$ | | **GROUND** |

## APPLICATIONS

The 27F256 flash-memory adds electrical chip-erasure and reprogrammability to EPROM non-volatility and ease of use. As such, the 27F256 is ideal for storing code or data-tables in embedded control applications where periodic updates are required.

The need for code updates pervades all phases of a system's life—from prototyping to system manufacture to after-sale service. In the factory, during prototyping, revisions to control code necessitate ultraviolet erasure and reprogramming of EPROM-based prototype codes. The 27F256 replaces the 15- to 20-minute ultraviolet erasure with one-second electrical erasure. Electrical chip-erasure and reprogramming occur in the same workstation or PROM-programmer socket.

Diagnostics, performed at subassembly or final assembly stages, often require the socketing of EPROMs. Socketed test codes are ultimately replaced with EPROMs containing the final program. With electrical chip-erasure and reprogramming, the 27F256 is soldered to the circuit board. Test codes are programmed into the 27F256 as it resides on the circuit board. Ultimately, the final code can be downloaded to the device. The 27F256's in-circuit alterability eliminates unnecessary handling and less-reliable socketed connections, while adding greater test flexibility.

Material and labor costs associated with code changes increase at higher levels of system integration—the most costly being code updates after sale. Code "bugs", or the desire to augment system functionality, prompt after-sale code updates. Field revisions to EPROM-based code require the removal of EPROM components or entire boards. The service technician performs the twenty-minute ultraviolet erasure and reprogramming on-site, or returns boards to the factory for rework. An alternate approach is to use one-time-programmable EPROMs. The service technician removes the "old" devices and replaces them with updated versions. The used components are discarded.

Designing with the in-circuit alterable 27F256 eliminates socketed memories, reduces overall material costs, and drastically cuts the labor costs associated with code updates. With the 27F256, code updates are implemented locally via an edge-connector, or remotely over a serial communication link.

A high degree of on-chip feature integration simplifies memory-to-processor interfacing. Figure 3 illustrates the interface between the MCS-51 microcontroller and one 27F256 flash-memory in a minimum chip-count system. Figure 4 depicts two 27F256s tied to the 80C186 system bus. In both instances, the 27F256's architecture minimizes interface circuitry needed for complete in-circuit updates of memory contents.

With cost-effective electrical erasure and reprogramming, the 27F256 fills the functionality gap between traditional EPROMs and EEPROMs. EPROM-compatible specifications, straightforward interfacing, and in-circuit alterability allows designers to easily augment memory flexibility and satisfy the need for updatable-code-storage in today's designs.

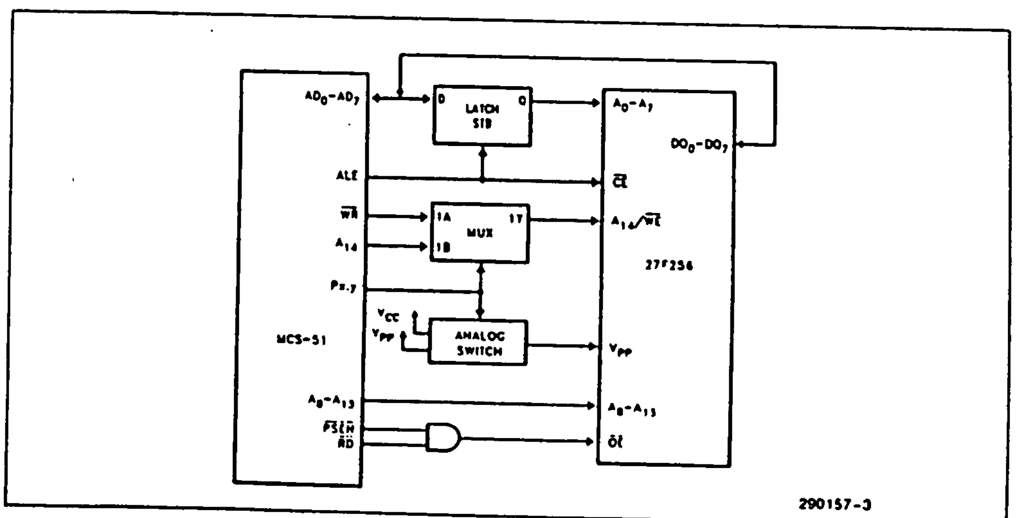


**Figure 3. 27F256 in an MCS-51 System**

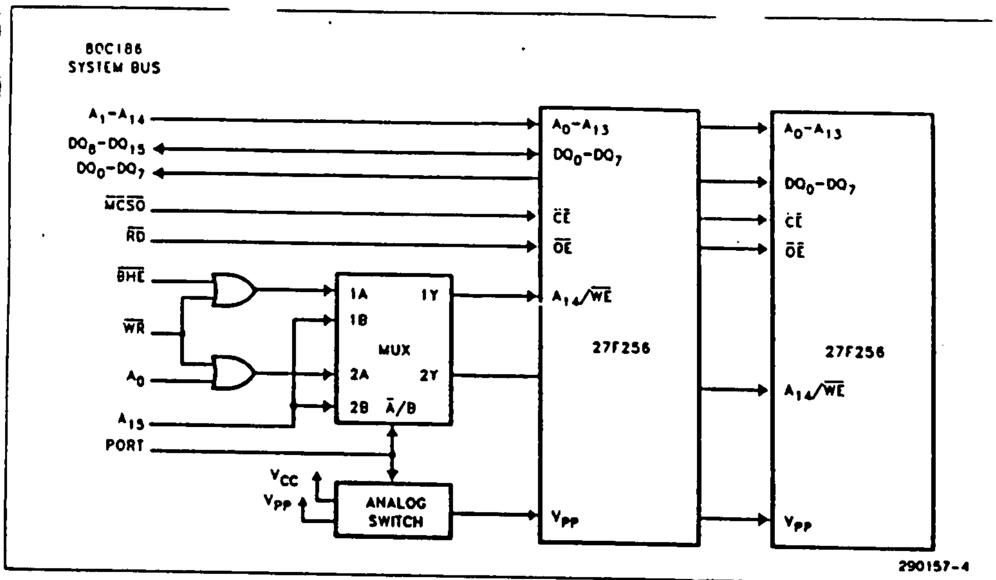


**Figure 4. 27F256 In an 80C186 System**

## PRINCIPLES OF OPERATION

Flash-memory augments EPROM functionality with in-circuit electrical erasure and reprogramming. The 27F256 introduces a command register to manage this new functionality. The command register allows for: 100% TTL-level control inputs; fixed power supplies during erasure and programming; and maximum EPROM compatibility.

In the absence of high voltage on the $V_{PP}$ pin, the 27F256 is a read-only memory. The 27F256 is completely read-compatible with the industry-standard 27256 and 27C256 EPROMs. Manipulation of the external memory-control pins yields the standard EPROM read, standby, output disable, and int$_e$ligent Identifier™ operations.

The same EPROM read, standby, and output disable operations are available when high voltage is applied to the $V_{PP}$ pin. In addition, high voltage on $V_{PP}$ enables erasure and programming of the device. All functions associated with altering memory contents—int$_e$ligent Identifier, erase, erase verify, program, and program verify—are accessed via the command register.

Commands are written to the register using standard microprocessor write timings. Register contents serve as input to an internal state-machine which controls the erase and programming circuitry. Write cycles also internally latch addresses and data needed for programming or erase operations. With the appropriate command written to the register, standard microprocessor read timings output array data, access the int$_e$ligent Identifier codes, or output data for erase and program verification.

Table 2. 27F256 Bus Operations

| | Operation (Pins) | $V_{PP}$ (1) | $A_0$ | $A_9$ | $\overline{CE}$ | $\overline{OE}$ | A14/ $\overline{WE}$ | $DQ_0$–$DQ_7$ |
|---|---|---|---|---|---|---|---|---|
| READ-ONLY | Read | $V_{PPL}$ | $A_0$ | $A_9$ | $V_{IL}$ | $V_{IL}$ | $A_{14}$ | Data Out |
| | Output Disable | $V_{PPL}$ | X | X | $V_{IL}$ | $V_{IH}$ | $V_{IH}$ | Tri-state |
| | Standby | $V_{PPL}$ | X | X | $V_{IH}$ | X | X | Tri-state |
| | Int$_e$ligent ID™ Manufacturer (2) | $V_{PPL}$ | $V_{IL}$ | $V_{ID}$ (3) | $V_{IL}$ | $V_{IL}$ | $V_{IL}$ | Data = 89H |
| | Int$_e$ligent ID™ Device (2) | $V_{PPL}$ | $V_{IH}$ | $V_{ID}$ (3) | $V_{IL}$ | $V_{IL}$ | $V_{IL}$ | Data = 91H |
| READ/WRITE | Read | $V_{PPH}$ | $A_0$ | $A_9$ | $V_{IL}$ | $V_{IL}$ | $V_{IH}$ | Data Out (4) |
| | Output Disable | $V_{PPH}$ | X | X | $V_{IL}$ | $V_{IH}$ | $V_{IH}$ | Tri-state |
| | Standby (5) | $V_{PPH}$ | X | X | $V_{IH}$ | X | X | Tri-state |
| | Write | $V_{PPH}$ | $A_0$ | $A_9$ | $V_{IL}$ | $V_{IH}$ | $V_{IL}$ | Data In (6) |

NOTES:
1. $V_{PPL}$ may be ground, a no-connect with a resistor tied to ground, or $\leq V_{CC}$ + 2.0V. $V_{PPH}$ is the programming voltage specified for the device. Refer to D.C. Characteristics. When $V_{PP} = V_{PPL}$, memory contents can be read but not written or erased.
2. Manufacturer and device codes may also be accessed via a command register write sequence. Refer to Table 3.
3. $11.5V \leq V_{ID} \leq 13.0V$.
4. Read operations with $V_{PP} = V_{PPH}$ may access array data or the Int$_e$ligent ID™.
5. With $V_{PP}$ at high voltage, the standby current equals Icc + Ipp (standby).
6. Refer to Table 3 for valid Data-In during a write operation.
7. X can be $V_{IL}$ or $V_{IH}$.

The command register is only alterable when $V_{PP}$ is at high voltage. Depending upon the application, the system designer may choose to make the $V_{PP}$ power supply switchable—available only when memory updates are desired. When high voltage is removed, the contents of the register default to the read command, making the 27F256 a read-only memory. Memory contents cannot be altered.

Write-Enable control is multiplexed with A14 to preserve compatibility with EPROM footprints. When $V_{PP}$ equals $V_{PPH}$, A14/Write-Enable functions as the Write-Enable pin. When $V_{PP}$ equals $V_{PPL}$, A14/Write-Enable is an address input line. The lowest order register bit contains the A14 information. In this manner, the 27F256 operates in a page-addressed fashion when $V_{PP}$ equals $V_{PPH}$.

The system designer may choose to "hard-wire" $V_{PP}$, making the high voltage supply constantly available. In this instance, all operations are performed in conjunction with the command register. The 27F256 is designed to accomodate either design practice, and to encourage optimization of the processor-memory interface.

## BUS OPERATIONS

### Read

The 27F256 has two control functions, both of which must be logically active, to obtain data at the outputs. Chip-Enable ($\overline{CE}$) is the power control and should be used for device selection. Output-Enable ($\overline{OE}$) is the output control and should be used to gate data from the output pins, independent of device selection. Figure 7 illustrates read timing waveforms.

The read operation only accesses array data when $V_{PP}$ is low ($V_{PPL}$). When $V_{PP}$ is high ($V_{PPH}$), the read operation can be used to access array data, to output the int$_e$ligent Identifier™ codes, and to access data for program/erase verification.

### Output Disable

With Output-Enable at a logic-high level ($V_{IH}$), output from the device is disabled. Output pins are placed in a high-impedance state.





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### Standby

With Chip-Enable at a logic-high level, the standby operation disables most of the 27F256's circuitry and substantially reduces device power consumption. The outputs are placed in a high-impedence state, independent of the Output-Enable signal. If the 27F256 is deselected during erasure, programming, or program/erase verification, the device draws active current until the operation is terminated.

### int$_{e}$ligent Identifier™

The int$_{e}$ligent Identifier operation outputs the manufacturer code (89H) and device code (91H). Programming equipment automatically matches the device with its proper erase and programming algorithms.

With Chip-Enable and Output-Enable at a logic low level, raising A9 to high voltage (11.5V–13.0V) activates the operation. Data read from locations 0000H and 0001H represent the manufacturer's code and the device code, respectively.

The manufacturer- and device-codes can also be read via the command register, for instances where the 27F256 is erased and reprogrammed in the target system. Following a write of 80H to the command register, a read from address location 0000H outputs the manufacturer code (89H). A read from address 0001H outputs the device code (91H).

### Write

Device erasure and programming are accomplished via the command register, when high voltage is applied to the $V_{PP}$ pin. The contents of the register serve as input to the internal state-machine. The state-machine outputs dictate the function of the device.

The command register itself does not occupy an addressable memory location. The register is a latch used to store the command, along with address and data information needed to execute the command. The command register is written by bringing Write-Enable to logic-low level ($V_{IL}$), while Chip-Enable is low. Addresses are latched on the falling edge of Write-Enable, while data is latched on the rising edge of the Write-Enable pulse. Standard microprocessor write timings are used.

The three high-order register bits (R7, R6, R5) encode the control functions. The lowest-order register bit (R0) contains the A14 information. All other register bits, R4 to R1, must be zero. The only exception is the reset command, when FFH is written to the register. Register bits R7–R0 correspond to data inputs D7–D0.

Refer to AC Write Characteristics and the Erase/Programming Waveforms for specific timing parameters.

## COMMAND DEFINITIONS

When low voltage is applied to the $V_{PP}$ pin, the contents of the command register default to 00H, enabling read-only operations. Placing high voltage on the $V_{PP}$ pin enables read/write operations. Device operations are selected by writing specific data patterns into the command register. Table 3 defines these 27F256 register commands.

### Read Command (Page 0/Page 1)

While $V_{PP}$ is high, for erasure and programming, memory contents can be accessed via the read command. When accessing array data with the read command, the A14 address information is written into bit zero (R0) of the command register. In effect, this divides the device into 16-kilobyte pages (page 0 and page 1).

The read operation (page 0) is initiated by writing 00H into the command register. Microprocessor read cycles retrieve array data from the lower 16-kilobyte page of memory. The device remains enabled for reads (page 0) until the command register contents are altered. By writing 01H to the command register, read cycles access data from the upper 16-kilobyte page (page 1) of memory.

The default contents of the register upon $V_{PP}$ power-up is 00H. This default value ensures that no spurious alteration of memory contents occurs during the $V_{PP}$ power transition. Where the $V_{PP}$ supply is hard-wired to the 27F256, the device powers-up and remains enabled for reads (page 0) until the command-register contents are changed. Refer to the AC Read Characteristics and Waveforms for specific timing parameters.

### Int$_{e}$ligent Identifier™ Command

Flash-memories are intended for use in applications where the local CPU alters memory contents. As such, manufacturer and device-codes must be accessible while the device resides in the target system. PROM programmers typically access signature codes by raising A9 to a high voltage. However, multiplexing high voltage onto address lines is not desired system-design practice.

**Table 3. Command Definitions**

| Command | Bus Cycles Req'd | First Bus Cycle | | | Second Bus Cycle | | |
|---|---|---|---|---|---|---|---|
| | | Operation(1) | Address(2) | Data(3) | Operation(1) | Address(2) | Data(3) |
| Read Memory | | | | | | | |
| a. Page 0 | 1 | Write | X | 00H | | | |
| b. Page 1 | 1 | Write | X | 01H | | | |
| Read Int$_e$ligent ID™ | 1 | Write | X | 80H | | | |
| Set-up Erase/Erase(4) | 2 | Write | X | 20H | Write | X | 20H |
| Erase Verify(4) | | | | | | | |
| a. Page 0 | 2 | Write | EA | A0H | Read | X | EVD |
| b. Page 1 | 2 | Write | EA | A1H | Read | X | EVD |
| Set-up Program/Program(5) | | | | | | | |
| a. Page 0 | 2 | Write | X | 40H | Write | PA | PD |
| b. Page 1 | 2 | Write | X | 41H | Write | PA | PD |
| Program Verify(5) | | | | | | | |
| a. Page 0 | 2 | Write | X | C0H | Read | X | PVD |
| b. Page 1 | 2 | Write | X | C1H | Read | X | PVD |
| Reset(6) | 2 | Write | X | FFH | Write | X | FFH |

NOTES:
1. Bus operations are defined in Table 2.
2. EA = Address of memory location to be read during erase verify.
   PA = Address of memory location to be programmed.
   Addresses are latched on the falling edge of the Write-Enable pulse.
3. EVD = Data read from location EA during erase verify.
   PD = Data to be programmed at location PA. Data is latched on the rising edge of Write-Enable.
   PVD = Data read from location PA during program verify. PA is latched on the Program command.
4. Figure 6 illustrates the Quick-Erase™ Algorithm.
5. Figure 5 illustrates the Quick-Pulse Programming™ Algorithm.
6. The second bus cycle must be followed by the desired command register write.

The 27F256 contains an int$_e$ligent Identifier™ operation to supplement traditional PROM-programming methodology. The operation is initiated by writing 80H into the command register. Following the command write, a read cycle from address 0000H retrieves the manufacturer code of 89H. A read cycle from address 0001H returns the device code of 91H. To terminate the operation, it is necessary to write another valid command into the register.

## Set-up Erase/Erase Commands

Set-up Erase is a command-only operation that stages the device for electrical erasure of all bytes in the array. The set-up erase operation is performed by writing 20H to the command register.

To commence chip-erasure, the erase command (20H) must again be written to the register. The erase operation begins with the rising edge of the Write-Enable pulse and terminates with the rising edge of the next Write-Enable pulse (i.e. Erase-Verify Command).

This two-step sequence of set-up followed by execution ensures that memory contents are not accidentally erased. Also, chip-erasure can only occur when high voltage is applied to the $V_{PP}$ pin. In the absence of this high voltage, memory contents are protected against erasure. Refer to AC Erase Characteristics and Waveforms for specific timing parameters.

## Erase-Verify Command (Page 0/Page 1)

The erase command erases all bytes of the array in parallel. After each erase operation, all bytes must

be verified. The erase verify opera- (page 0) is initiated by writing A0H into the command register. Erase verify (page 1) is started by writing A1H into the register. The address for the byte to be verified must be supplied as it is latched on the falling edge of the Write-Enable pulse. The register write terminates the erase operation with the rising edge of its Write-Enable pulse.

The 27F256 applies an internally-generated margin voltage to the addressed byte. Reading FFH from the addressed byte indicates that all bits in the byte are erased.

The erase-verify command must be written to the command register prior to each byte verification to latch its address. The process continues for each byte in the 16-kilobyte page until a byte does not return FFH data, or the last address in the page is accessed. The erase-verify (page 1) command must be written to the register to cross the page boundary.

In the case where FFH data is not read, another erase operation is performed. (Refer to Set-up Erase/Erase). Verification then resumes from the address of the last-verified byte. Once all bytes in the array have been verified, the erase step is complete. The device can be programmed. At this point, the verify operation is terminated by writing a valid command (e.g. Program Set-up) to the command register. Figure 6, the Flash-Erase™ Algorithm illustrates how commands and bus operations are combined to perform electrical erasure of the 27F256. Refer to AC Erase Characteristics and Waveforms for specific timing parameters.

### Set-up Program/Program Commands (Page 0/Page 1)

Set-up program is a command-only operation that stages the device for byte programming. Writing 40H (page 0) or 41H (page 1) into the command register performs the set-up operation. The register write latches the A14 information into bit zero (R0) of the register to select the desired 16-kilobyte page.

Once the program set-up operation is performed, the next Write-Enable pulse causes a transition to an active programming operation. Addresses are internally latched on the falling edge of the Write-Enable pulse. Data is internally latched on the rising edge of the Write-Enable pulse. The rising edge of Write-Enable also begins the programming operation. The programming operation terminates with the next rising edge of Write-Enable, used to write the program-verify command. Refer to AC Programming Characteristics and Waveforms for specific timing parameters.

### Program-Verify Command (Page 0/Page 1)

The 27F256 is programmed on a byte-by-byte basis. Byte programming may occur sequentially or at random. Following each programming operation, the byte just programmed must be verified.

The program-verify operation (page 0) is initiated by writing C0H into the command register. Program verify (page 1) is entered by writing C1H into the register. Bit zero (R0) of the register represents A14, selecting one of the two 16-kilobyte pages. The register write terminates the programming operation with the rising edge of its Write-Enable pulse. The program-verify operation stages the device for verification of the byte last programmed. No new address information is latched.

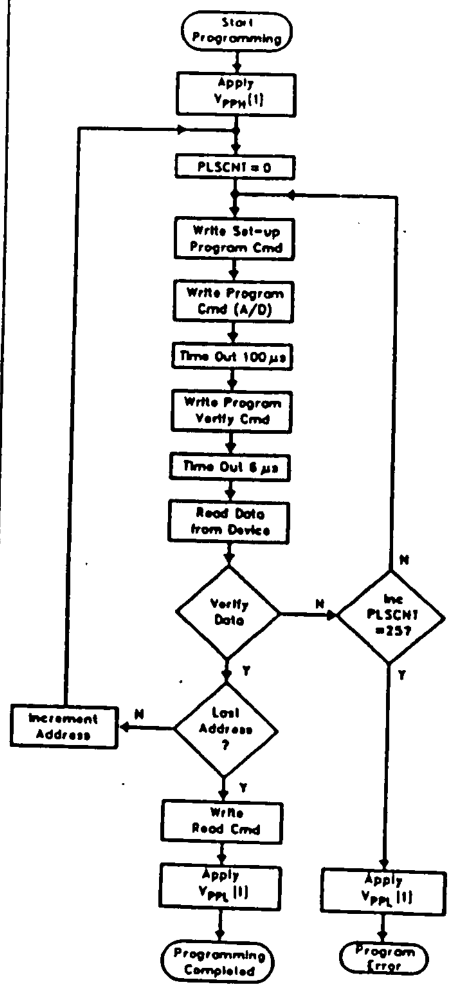
The 27F256 applies an internally-generated margin voltage to the byte. A microprocessor read cycle outputs the data. A successful comparison between the programmed byte and true data means that the byte is successfully programmed. Programming then proceeds to the next desired byte location. Figure 5, the 27F256 Quick-Pulse Programming™ Algorithm, illustrates how commands are combined with bus operations to perform byte programming. Refer to AC Programming Characteristics and Waveforms for specific timing parameters.

### Reset Command

A reset command is provided as a means to safely abort the erase- or program-command sequences. Following either set-up command (erase or program) with two consecutive writes of FFH will safely abort the operation. Memory contents will not be altered. A valid command must then be written to place the device in the desired state.

## QUICK-PULSE PROGRAMMING™ ALGORITHM

The Quick-Pulse Programming™ algorithm uses programming operations of 100 microsecond duration. Each operation is followed by a byte verification to determine when the addressed byte has been successfully programmed. The algorithm allows for up to 25 programming operations per byte, although most bytes verify on the first or second operation. The entire sequence of programming and byte verification is performed with $V_{PP}$ at high voltage. Figure 5 illustrates the Quick-Pulse Programming algorithm.

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| Bus Operation | Command | Comments |
|---|---|---|
| Standby | | Wait for $V_{PP}$ Ramp to $V_{PPH}$ (1) |
| | | Initialize Pulse-Count |
| Write | Set-up Program | Data = 40H/41H |
| Write | Program | Valid Address/Data |
| Standby | | Duration of Program Operation ($t_{WHWH1}$) |
| Write | Program Verify(2) | Data = C0H/C1H; Stops Program Operation |
| Standby | | $t_{WHGL}$ |
| Read | | Read Byte to Verify Programming |
| Standby | | Compare Data Output to Data Expected |
| Write | Read | Data = 00H, Resets the Register for Read Operations |
| Standby | | Wait for $V_{PP}$ Ramp to $V_{PPL}$ (1) |

**NOTES:**

1. See D.C. Characteristics for value of $V_{PPH}$. The $V_{PP}$ power supply can be hard-wired to the device or switchable. When $V_{PP}$ is switched, $V_{PPL}$ may be ground, no-connect with a resistor tied to ground, or less than $V_{CC}$ + 2.0V. Refer to Principles of Operation.
2. Program Verify is only performed after byte programming. A final read/compare may be performed (optional) after the register is written with the Read command.

**Figure 5. 27F256 Quick-Pulse Programming™ Algorithm**

## QUICK-ERASE™ ALGORITHM

ntel's Quick-Erase algorithm yields fast and reliable lectrical erasure of memory contents. The algo- ithm employs a closed-loop flow, similar to the Quick-Pulse Programming™ algorithm, to simulta- eously remove charge from all bits in the array.

rasure begins with a read of memory contents. The 7F256 is erased when shipped from the factory. leading FFH data from the device would immedi- tely be followed by device programming.

niform and reliable erasure is ensured by first pro- amming all bits in the device to their charged state Data = 00H). This is accomplished, using the uick-Pulse Programming algorithm, in approxi- ately four seconds.

rase execution then continues with an initial erase peration. Erase verification (data = FFH) begins at ddress 0000H and continues through the array to he last address, or until data other than FFH is en- ountered. With each erase operation, an increasing umber of bytes verify to the erased state. Erase fficiency may be improved by storing the address of he last byte verified in a register. Following the next rase operation, verification starts at that stored ad- dress location. A total of sixty-four erase operations are allowed, which corresponds to approximately ten seconds of cumulative erase time. Erasure typi- cally occurs in one second. Figure 6 illustrates the Quick-Erase Algorithm.

## DESIGN CONSIDERATIONS

### Two-Line Output Control

Flash-memories are often used in larger memory ar- rays. Intel provides two read-control inputs to acco- modate multiple memory connections. Two-line con- trol provides for:

a) the lowest possible memory power dissipation, and

b) complete assurance that output bus contention will not occur.

To efficiently use these two control inputs, an ad- dress-decoder output should drive chip-enable, while the system's read signal controls all flash- memories and other parallel memories. This assures that only enabled memory devices have active out- puts, while deselected devices maintain the low power standby condition.

### Power Supply Decoupling

Flash-memory power-switching characteristics re- quire careful device decoupling. System designers are interested in three supply current ($I_{CC}$) issues– standby, active and transient current peaks pro- duced by falling and rising edges of Chip-Enable. The capacitive and inductive loads on the device outputs determine the magnitudes of those peaks.

Two-line control and proper decoupling capacitor selection will supress transient voltage peaks. Each device should have a 0.1μF ceramic capacitor con- nected between $V_{CC}$ and $V_{SS}$, and between $V_{PP}$ and $V_{SS}$.

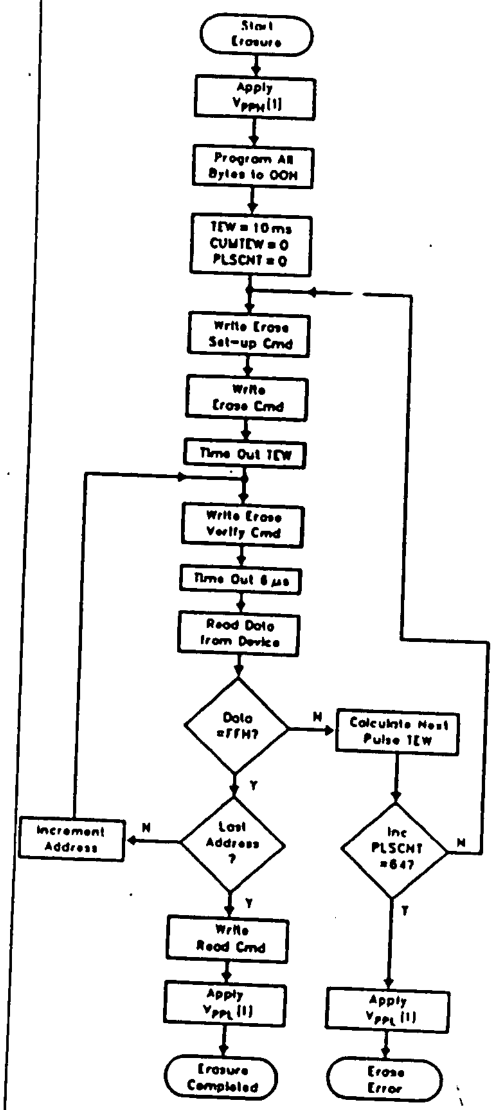
Place the high-frequency, low-inherent-inductance capacitors as close as possible to the devices. Also, for every eight devices, a 4.7μF electrolytic capaci- tor should be placed at the array's power supply connection, between $V_{CC}$ and $V_{SS}$. The bulk capaci- tor will overcome voltage slumps caused by printed- circuit-board trace inductance, and will supply charge to the smaller capacitors as needed.

### $V_{PP}$ Trace on Printed Circuit Boards

Programming flash-memories, while they reside in the target system, requires that the printed circuit board designer pay attention to the $V_{PP}$ power sup- ply trace. The $V_{PP}$ pin supplies the memory cell cur- rent for programming. Use similar trace width and layout considerations given the $V_{CC}$ power bus. Ad- equate $V_{PP}$ supply traces and decoupling will de- crease $V_{PP}$ voltage spikes and overshoots.

### Power Up/Down Sequencing

The 27F256 is designed to offer protection against accidental erasure or programming, caused by spuri- ous system-level signals that may exist during power transitions. The 27F256 powers-up in its read-only state. Also, with its control register architecture, al- teration of memory contents only occurs after suc- cessful completion of the two-step command se- quences. While these precautions are sufficient for most applications, it is recommended that $V_{CC}$ reach its steady-state value before raising $V_{PP}$ above $V_{CC}$ + 2.0V. In addition, upon powering-down, $V_{PP}$ should be below $V_{CC}$ + 2.0V, before lowering $V_{CC}$.



290157-6

| Bus Operation | Command | Comments |
|---|---|---|
| Standby | | Wait for $V_{PP}$ Ramp to $V_{PPH}$(1) |
| | | Use Quick-Pulse Programming™ Algorithm (Fig.5) |
| | | Initialize: Erase Time Cum Erase Time Pulse-Count |
| Write | Set-up Erase | Data = 20H |
| Write | Erase | Data = 20H |
| Standby | | Duration of Erase; Operation ($t_{WHWH2}$) |
| Write | Erase Verify(2) | Addr = Byte to Verify; Data = A0H/A1H; Stops Erase Operation |
| Standby | | $t_{WHGL}$ |
| Read | | Read Byte to Verify Erasure |
| Standby | | Compare Output to FFH CUMTEW = CUMTEW + TEW TEW = Integer Divide INT(CUMTEW/8) |
| Write | Read | Data = 00H, Reset the Register for Read Operations |
| Standby | | Wait for $V_{PP}$ Ramp to $V_{PPL}$(1) |

NOTES:
1. See D.C. Characteristics for value of $V_{PPH}$. The $V_{PP}$ power supply can be hard-wired to the device or switchable. When $V_{PP}$ is switched, $V_{PPL}$ may be ground, no-connect with a resistor tied to ground, or less than $V_{CC}$ + 2.0V. Refer to Principles of Operation.
2. Erase Verify is performed only after chip-erasure. A final read/compare may be performed (optional) after the register is written with the read command.

**Figure 6. 27F256 Quick-Erase™ Algorithm**

intel

ISOLUTE MAX
erating Temperatur
During Read .....
During Erase/Progr
mperature Under B
rage Temperature
tage on Any Pin w
Respect to Ground
tage on Pin $A_9$ wit
Respect to Ground
Supply Voltage w
Respect to Ground
During Erase/Progr
C Supply Voltage w
Respect to Ground
tput Short Circuit C

TES:
Operating temperatur
Minimum D.C. input v
ximum D.C. voltage
Maximum D.C. voltag
Output shorted for no

PERATING CC

| Symbol | |
|---|---|
| $T_A$ | Op |
| $V_{CC}$ | Vc |

D.C. CHARACTI

| Symbol | |
|---|---|
| $I_{LI}$ | Inpu |
| $I_{LO}$ | Outp |
| $I_{CCS}$ | $V_{CC}$ |
| $I_{CC1}$ | $V_{CC}$ |
| $I_{CC2}$ | $V_{CC}$ |

## ABSOLUTE MAXIMUM RATINGS

Operating Temperature
During Read .................. 0°C to + 70°C(1)
During Erase/Program ........... 0°C to + 70°C

Temperature Under Bias ......... − 10°C to + 80°C

Storage Temperature .......... − 65°C to + 125°C

Voltage on Any Pin with
Respect to Ground .......... − 2.0V to + 7.0V(2)

Voltage on Pin $A_9$ with
Respect to Ground ....... − 2.0V to + 13.5V(2,3)

$V_{PP}$ Supply Voltage with
Respect to Ground
During Erase/Program .... − 2.0V to + 14.0V(2,3)

$V_{CC}$ Supply Voltage with
Respect to Ground .......... − 2.0V to + 7.0V(2)

Output Short Circuit Current............. 100 mA(4)

**Notice: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*

*NOTICE: Specifications contained within the following tables are subject to change.*

NOTES:
1. Operating temperature is for commercial product defined by this specification.
2. Minimum D.C. input voltage is − 0.5V. During transitions, inputs may undershoot to − 2.0V for periods less than 20ns. Maximum D.C. voltage on output pins is $V_{CC}$ + 0.5V, which may overshoot to $V_{CC}$ + 2.0V for periods less than 20ns.
3. Maximum D.C. voltage on Aq or $V_{PP}$ may overshoot to + 14.0V for periods less than 20 ns.
4. Output shorted for no more than one second. No more than one output shorted at a time.

## OPERATING CONDITIONS

| Symbol | Parameter | Limits | | Unit | Comments |
|---|---|---|---|---|---|
| | | Min | Max | | |
| $T_A$ | Operating Temperature | 0 | 70 | °C | For Read-Only and Read/Write Operations |
| $V_{CC}$ | $V_{CC}$ Supply Voltage | 4.50 | 5.50 | V | |

## D.C. CHARACTERISTICS—TTL/NMOS COMPATIBLE

| Symbol | Parameter | Limits | | Unit | Test Conditions |
|---|---|---|---|---|---|
| | | Min | Max | | |
| $I_{LI}$ | Input Leakage Current | | ± 1.0 | μA | $V_{CC}$ = $V_{CC}$ max<br>$V_{IN}$ = $V_{CC}$ or $V_{SS}$ |
| $I_{LO}$ | Output Leakage Current | | ± 1.0 | μA | $V_{CC}$ = $V_{CC}$ max<br>$V_{OUT}$ = $V_{CC}$ or $V_{SS}$ |
| $I_{CCS}$ | $V_{CC}$ Standby Current | | 1.0 | mA | $V_{CC}$ = $V_{CC}$ max<br>$\overline{CE}$ = $V_{IH}$ |
| $I_{CC1}$ | $V_{CC}$ Active Read Current | | 30 | mA | $V_{CC}$ = $V_{CC}$ max $\overline{CE}$ = $V_{IL}$<br>f = 6MHz, $I_{OUT}$ = 0 mA |
| $I_{CC2}$ | $V_{CC}$ Programming Current | | 30 | mA | $\overline{CE}$ = $V_{IL}$<br>Programming in progress |

## D.C. CHARACTERISTICS—TTL/NMOS COMPATIBLE (Continued)

| Symbol | Parameter | Limits Min | Limits Max | Unit | Test Conditions |
|---|---|---|---|---|---|
| $I_{CC3}$ | $V_{CC}$ Erase Current | | 30 | mA | $\overline{CE} = V_{IL}$ Erasure in progress |
| $I_{PPS}$ | $V_{PP}$ Standby Current | | 1.0 | µA | $V_{PP} = V_{PPL}$ |
| $I_{PP1}$ | $V_{PP}$ Read Current | | 200 | µA | $V_{PP} = V_{PPH}$ |
| $I_{PP2}$ | $V_{PP}$ Programming Current | | 30 | mA | $V_{PP} = V_{PPH}$ Programming in progress |
| $I_{PP3}$ | $V_{PP}$ Erase Current | | 30 | mA | $V_{PP} = V_{PPH}$ Erasure in progress |
| $V_{IL}$ | Input Low Voltage | −0.5 | 0.8 | V | |
| $V_{IH}$ | Input High Voltage | 2.0 | $V_{CC}$ + 0.5 | V | |
| $V_{OL}$ | Output Low Voltage | | 0.45 | V | $I_{OL} = 2.1$ mA $V_{CC} = V_{CC}$ min |
| $V_{OH1}$ | Output High Voltage | 2.4 | | V | $I_{OH} = -2.5$ mA $V_{CC} = V_{CC}$ min |
| $V_{ID}$ | $A_9$ int$_e$ligent Identifier™ Voltage | 11.50 | 13.00 | V | $A_9 = V_{ID}$ |
| $I_{ID}$ | $A_9$ int$_e$ligent Identifier™ Current | | 500 | µA | $A_9 = V_{ID}$ |
| $V_{PPL}$ | $V_{PP}$ during Read-Only Operations | 0.00 | $V_{CC}$ + 2.0V | V | Note: Erase/Program are inhibited when $V_{PP} = V_{PPL}$ |
| $V_{PPH}$ | $V_{PP}$ during Read/Write Operations | 12.50 | 13.00 | V | |

## D.C. CHARACTERISTICS—CMOS COMPATIBLE

| Symbol | Parameter | Limits Min | Limits Max | Unit | Test Conditions |
|---|---|---|---|---|---|
| $I_{LI}$ | Input Leakage Current | | ± 1.0 | µA | $V_{CC} = V_{CC}$ max $V_{IN} = V_{CC}$ or $V_{SS}$ |
| $I_{LO}$ | Output Leakage Current | | ± 1.0 | µA | $V_{CC} = V_{CC}$ max $V_{OUT} = V_{CC}$ or $V_{SS}$ |
| $I_{CCS}$ | $V_{CC}$ Standby Current | | 100 | µA | $V_{CC} = V_{CC}$ max $\overline{CE} = V_{IH}$ |

## D.C. CHARACTERISTICS—CMOS COMPATIBLE (Continued)

| Symbol | Parameter | Limits Min | Limits Max | Unit | Test Conditions |
|---|---|---|---|---|---|
| $I_{CC1}$ | $V_{CC}$ Active Read Current | | 20 | mA | $V_{CC} = V_{CC}$ max $\overline{CE} = V_{IL}$ $f = 6MHz$, $I_{OUT} = 0$ mA |
| $I_{CC2}$ | $V_{CC}$ Programming Current | | 30 | mA | $\overline{CE} = V_{IL}$ Programming in progress |
| $I_{CC3}$ | $V_{CC}$ Erase Current | | 30 | mA | $\overline{CE} = V_{IL}$ Erasure in progress |
| $I_{PPS}$ | $V_{PP}$ Standby Current | | 1.0 | µA | $V_{PP} = V_{PPL}$ |
| $I_{PP1}$ | $V_{PP}$ Read Current | | 200 | µA | $V_{PP} = V_{PPH}$ |
| $I_{PP2}$ | $V_{PP}$ Programming Current | | 30 | mA | $V_{PP} = V_{PPH}$ Programming in progress |
| $I_{PP3}$ | $V_{PP}$ Erase Current | | 30 | mA | $V_{PP} = V_{PPH}$ Erasure in progress |
| $V_{IL}$ | Input Low Voltage | −0.5 | 0.8 | V | |
| $V_{IH}$ | Input High Voltage | 0.7 $V_{CC}$ | $V_{CC}$ + 0.5 | V | |
| $V_{OL}$ | Output Low Voltage | | 0.45 | V | $I_{OL} = 2.1$ mA $V_{CC} = V_{CC}$ min |
| $V_{OH1}$ | Output High Voltage | 0.85 $V_{CC}$ | | V | $I_{OH} = -2.5$ mA $V_{CC} = V_{CC}$ min |
| $V_{OH2}$ | | $V_{CC}$ − 0.4 | | | $I_{OH} = -100$ µA $V_{CC} = V_{CC}$ min |
| $V_{ID}$ | $A_9$ intelligent Identifier™ Voltage | 11.50 | 13.00 | V | $A_9 = V_{ID}$ |
| $I_{ID}$ | $A_9$ intelligent Identifier™ Current | | 500 | µA | $A_9 = V_{ID}$ |
| $V_{PPL}$ | $V_{PP}$ during Read-Only Operations | 0.00 | $V_{CC}$ + 2.0 | V | Note: Erase/Program are inhibited when $V_{PP} = V_{PPL}$ |
| $V_{PPH}$ | $V_{PP}$ during Read/Write Operations | 12.50 | 13.00 | V | |

CAPACITANCE(1) $T_A = 25°C$, $f = 1.0$ MHz

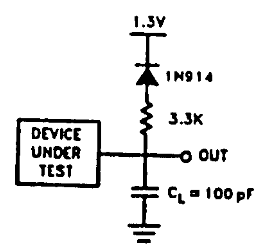
| Symbol | Parameter | Limits Min | Limits Max | Unit | Conditions |
|---|---|---|---|---|---|
| $C_{IN}$ | Address/Control Capacitance | | 6 | pF | $V_{IN} = 0V$ |
| $C_{OUT}$ | Output Capacitance | | 12 | pF | $V_{OUT} = 0V$ |

NOTE:
1. Sampled, not 100% tested.

### A.C. TEST CO[illegible]IONS

Input Rise and Fall Times (10% to 90%) ...... 10 ns
Input Pulse Levels ............... $V_{OL}$ and $V_{OH}$
Input Timing Reference Level .......... $V_{IL}$ and $V_{IH}$
Output Timing Reference Level ........ $V_{IL}$ and $V_{IH}$

### A.C. TESTING LOAD CIRCUIT

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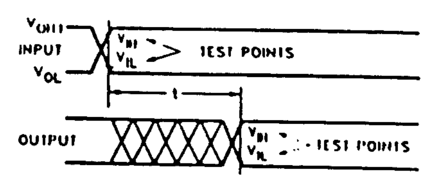
$C_L$ = 100 pF
$C_L$ Includes Jig Capacitance

### A.C. TESTING INPUT/OUTPUT WAVEFORM

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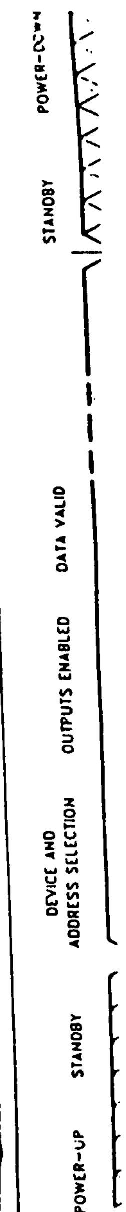
A.C Testing: Inputs are driven at $V_{OH}$ for a logic "1" and $V_{OL}$ for a logic "0". Testing measurements are made at $V_{IH}$ for a logic "1" and $V_{IL}$ for a logic "0". Rise/Fall time ≤ 10 ns.

## A.C. CHARACTERISTICS—READ-ONLY OPERATIONS

| Versions | | 27F256-170P2C2 | | 27F256-200P2C2 | | 27F256-250P2C2 | | Unit |
|---|---|---|---|---|---|---|---|---|
| Symbol | Characteristics | Min | Max | Min | Max | Min | Max | |
| $t_{AVAV}/t_{RC}$ | Read Cycle Time | 170 | | 200 | | 250 | | ns |
| $t_{ELQV}/t_{CE}$ | Chip Enable Access Time | | 170 | | 200 | | 250 | ns |
| $t_{AVQV}/t_{ACC}$ | Address Access Time | | 170 | | 200 | | 250 | ns |
| $t_{GLQV}/t_{OE}$ | Output Enable Access Time | | 70 | | 75 | | 80 | ns |
| $t_{ELQX}/t_{LZ}$ | Chip Enable to Output in Low Z | 0 | | 0 | | 0 | | ns |
| $t_{EHQZ}$ | Chip Enable to Output in High Z | | 55 | | 60 | | 65 | ns |
| $t_{GLQX}/t_{OLZ}$ | Output Enable to Output in Low Z | 0 | | 0 | | 0 | | ns |
| $t_{GHQZ}/t_{DF}$ | Output Disable to Output in High Z | | 35 | | 45 | | 55 | ns |
| $t_{OH}$ | Output Hold from Address, $\overline{CE}$, or $\overline{OE}$ Change (1) | 0 | | 0 | | 0 | | ns |
| $t_{WHGL}$ | Write Recovery Time Before Read | 6 | | 6 | | 6 | | ns |

NOTES:
1. Whichever occurs first.
2. Rise/Fall times ≤ 10 ns.



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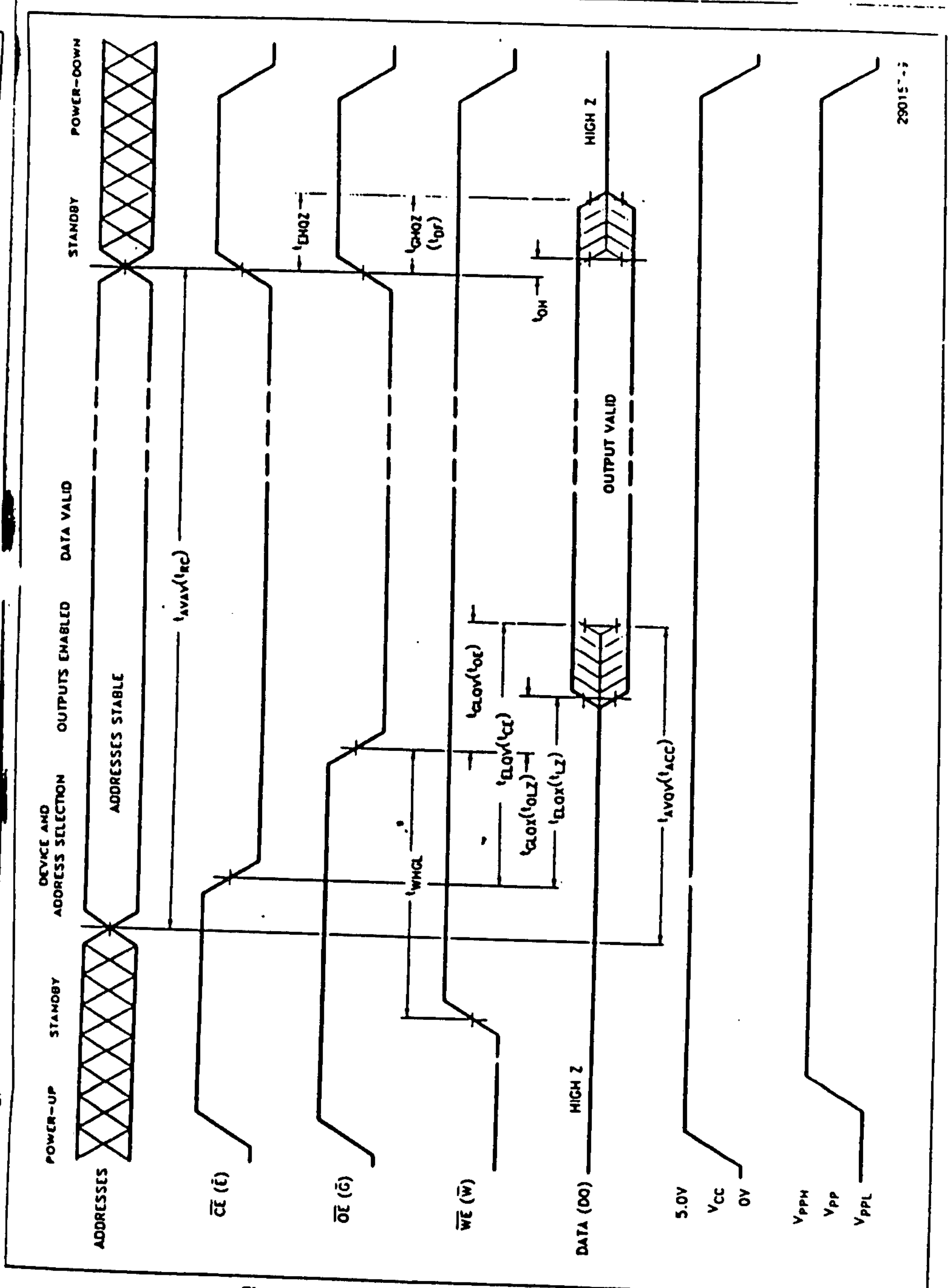



**Figure 7. AC Waveforms for Read Operations**

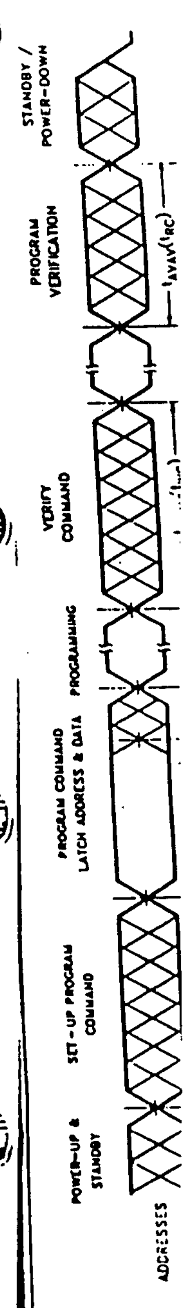
## A.C. CHARACTERISTICS—For Write/Erase/Program Operations[1]

| Versions | | 27F256-170P2C2 | | 27F256-200P2C2 | | 27F256-250P2C2 | | Unit |
|---|---|---|---|---|---|---|---|---|
| Symbol | Characteristics | Min | Max | Min | Max | Min | Max | |
| $t_{AVAV}/t_{WC}$ | Write Cycle Time | 170 | | 200 | | 250 | | ns |
| $t_{AVWL}/t_{AS}$ | Address Set-up Time | 0 | | 0 | | 0 | | ns |
| $t_{WLAX}/t_{AH}$ | Address Hold Time | 60 | | 75 | | 90 | | ns |
| $t_{DVWH}/t_{DS}$ | Data Set-up Time | 50 | | 50 | | 50 | | ns |
| $t_{WHDX}/t_{DH}$ | Data Hold Time | 10 | | 10 | | 10 | | ns |
| $t_{WHGL}$ | Write Recovery Time Before Read | 6 | | 6 | | 6 | | µs |
| $t_{GHWL}$ | Read Recovery Time Before Write | 0 | | 0 | | 0 | | µs |
| $t_{ELWL}/t_{CS}$ | Chip Enable Set-up Time | 0 | | 0 | | 0 | | ns |
| $t_{WHEH}/t_{CH}$ | Chip Enable Hold Time | 0 | | 0 | | 0 | | ns |
| $t_{WLWH}/t_{WP}$ | Write Pulse Width | 50 | | 60 | | 75 | | ns |
| $t_{WHWL}/t_{WPH}$ | Write Pulse Width High | 50 | | 60 | | 75 | | ns |
| $t_{WHWH1}$ | Programming Operation | 95 | 150 | 95 | 150 | 95 | 150 | µs |
| $t_{WHWH2}$ | Erase Operation | (2) | (2) + 5% | (2) | (2) + 5% | (2) | (2) + 5% | |
| $t_{EHVP}$ | Chip Enable Set-up Time to $V_{PP}$ Ramp | 100 | | 100 | | 100 | | ns |
| $t_{VPEL}$ | $V_{PP}$ Set-up Time to Chip Enable Low | 100 | | 100 | | 100 | | ns |

NOTES:
1. Read timing characteristics during read/write operations are the same as during read-only operations. Refer to A.C. Characteristics for Read-Only Operations.
2. The duration of each erase operation is variable and is calculated in the Quick-Erase™ Algorithm. The duration of the current erase operation is equal to the truncated value of cumulative erase time divided by eight (integer divide).

TEW = Integer Divide (CUMTEW/8)

The duration of the erase operation actually applied can exceed the calculated value by a maximum tolerance of 5%. Refer to Figure 6 for additional details.



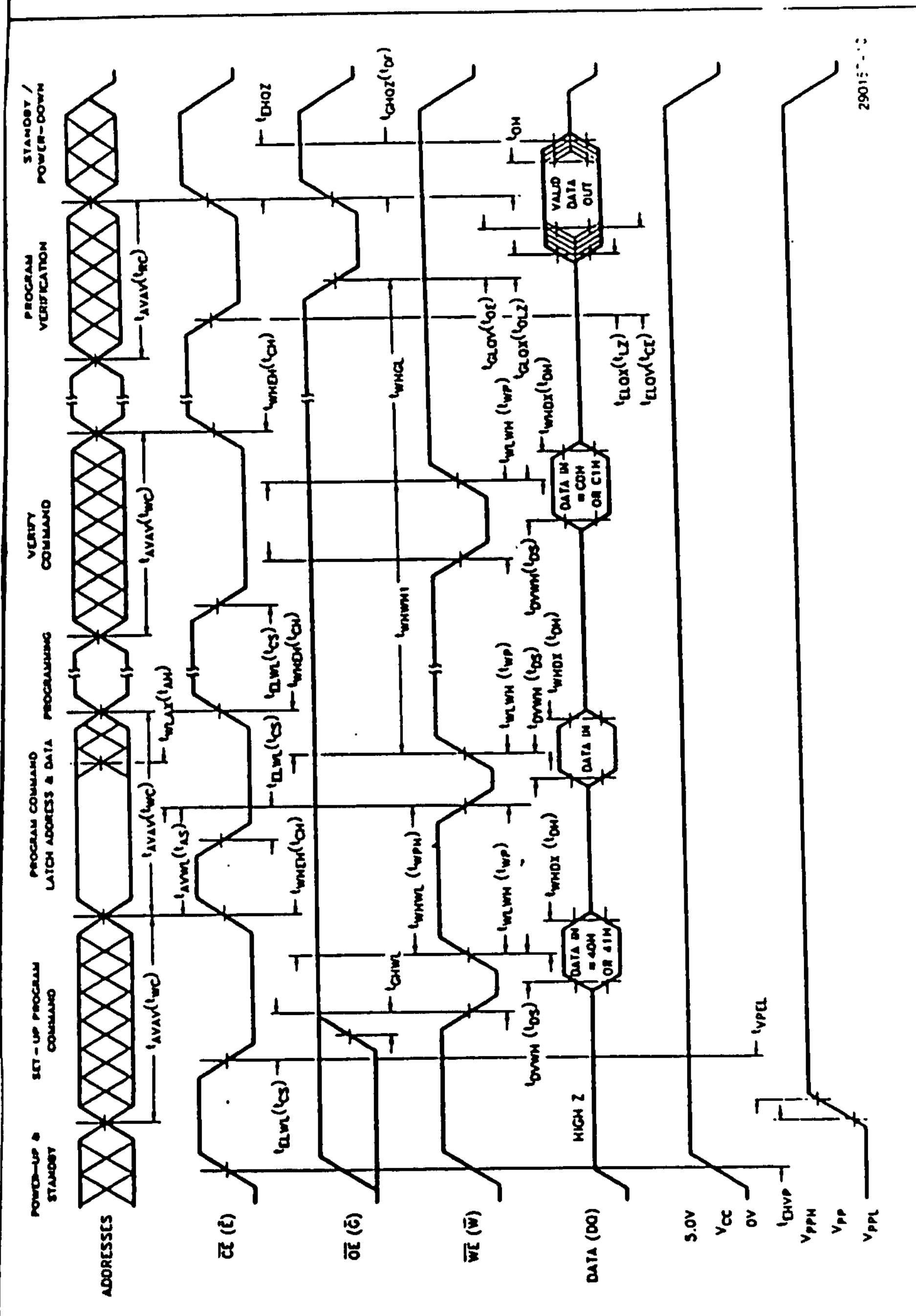



Figure 8. A.C. Waveforms for Programming Operations

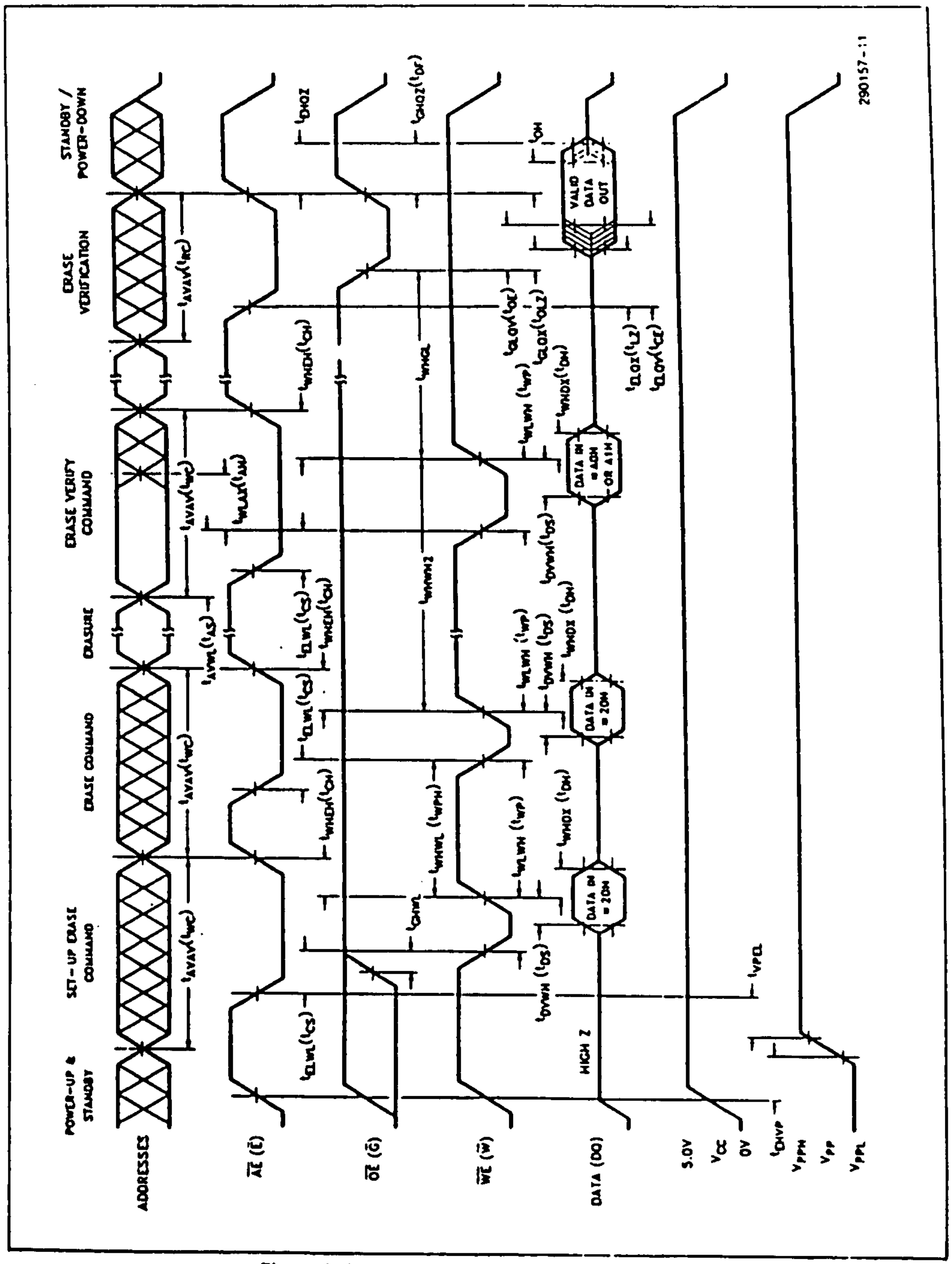



Figure 9. A.C. Waveforms for Erase Operations

intel

ORDERING

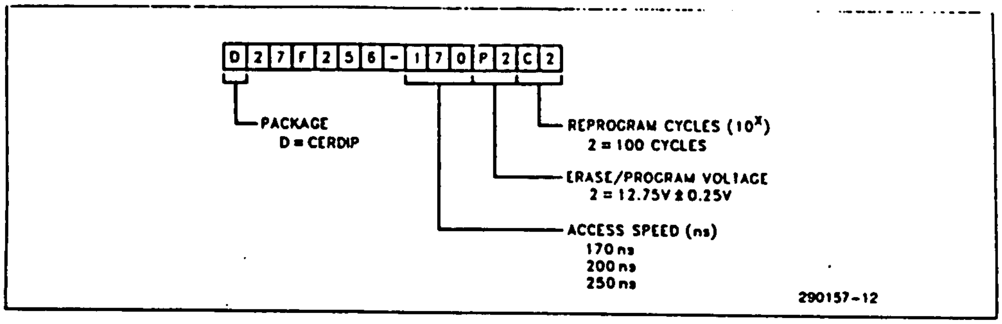
VALID COMB

D27F256-17

D27F256-20

D27F256-25

## ORDERING INFORMATION




VALID COMBINATIONS:
D27F256-170P2C2
D27F256-200P2C2
D27F256-250P2C2